REMARKS

Present Status of the Application

In response to the Second Office Action dated **Sep. 17, 200**, Applicants respectfully request consideration of the following discussion on the rejection to the pending claims. No claims have been canceled, no claims have been added, and no claims have been amended. Accordingly, Claims 1-16 remain pending in the present application.

In the third Office Action, the Office Action rejected Claims 1-9 under 35 U.S.C. §103(a) as being unpatentable over Ziegler. The Office Action also rejected Claims 10, 12 and 13 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Handy "The Cache Memory Book" (Handy).

The Examiner also indicated that claim 11 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Examiner further indicated that claims 14-16 were allowed. Applicants appreciate this indication of allowable subject matter.

Concerning The Rejection Of Claims 1-9 Under 35 U.S.C. §103(A) As Being Unpatentable Over Ziegler

Applicants respectfully submit that claim 1 patently defines over the cited prior art for at least the reasons stated in the response to the previous office action, and further in view of the reasons set forth as followed.

The Office Action restated that claim 1 is being rejected by Ziegler because "a cache is a specialized buffer therefore Ziegler's cache reads on Applicants' buffer." In addition, even the Ziegler does not disclose the "peripheral device interface controller installed within the control chip," however, it is well known in the art the benefit for incorporation of separate modules that are in direct communication on the same chip.

Regarding The Cache 166 Of Figure 2 In Ziegler

Applicants do not agree with the assertions. The Office action, in response to the Amendment, cited a WordNet definition of a cache as "RAM memory that is set aside as a specialized buffer storage that is continually updated; used to optimize data transfers between system elements with different characteristics" and concluded that a cache is a specialized buffer therefore Ziegler's cache reads on Applicants' buffer. However, the "data buffer" defined in the claim 1 is totally different from the "element 166" of figure 2 in Ziegler.

As defined in claim 1, "a data buffer located within the control chip for holding a data stream read from the memory unit so that **data required by the peripheral device bus are provided**", the data stream holding in the data buffer is required by the **peripheral device bus**. However, regarding the cache 166 of figure 2 in Ziegler, the **memory cache 166** is used for the **coherent transaction check, instead of data for the peripheral device bus**. As stated in col.11, lines 42-55 in Ziegler, "**in FIFO order,** coherent transactions stored in CCC queues 164 and 168 are checked against memory caches 166 and 170, respectively." The memory caches

166 and 170 of the memory modules, in Ziegler, are **used for the CPU being relieved of the task of sending cache coherency checking requests to the various modules**.

Regarding the definition of the "Cache", as defined in the IEEE The Authoritative Dictionary of IEEE Standards Terms, attached herewith for reference, a cache is "(1) A buffer inserted between **one or more processors** and **the bus**, used to hold currently active copies of the blocks from main memory. (2) A small portion of high-speed memory used for temporary storage of frequency-used data, instructions, or operations." Furthermore, a cache memory is defined as "(1) A buffer memory inserted between **one or more processors** and **the bus**, which is used to hold currently active copies of blocks of information from main memory. (2) A buffer memory inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. Cache memories exploit spatial locality by what is brought into a cache. Temporal locality is exploited by the strategy employed for determining what is removed from the cache." In according to the definition in the IEEE The Authoritative Dictionary of IEEE Standards Terms, the "data buffer" located within the control chip for holding a data stream read from the memory unit so that **data required by the peripheral device bus are provided**, which is different from the cache 166 of figure 2 in Ziegler, for **the CPU being relieved of the task of sending cache coherency checking requests.**

Regarding The Controller Subelement Within Element 114 Of Figure 2 In Ziegler

Regarding that the Ziegler does not disclose the "peripheral device interface controller installed within the control chip," however, the Office action asserted that it is well known in the art the benefit for incorporation of separate modules that are in direct communication on the same chip. Applicants do not agree with the assertions.

As stated in col.11, lines 42-55 in Ziegler, "in FIFO order, coherent transactions stored in CCC queues 164 and 168 are checked against memory caches 166 and 170, respectively. In FIFO order, coherent transactions stored in CCC queues 164 and 168 are checked against memory caches 166 and 170, respectively, and **the results are reported to main memory controller 114** on lines 152 and 142, respectively. The results are stored on the scoreboard until all modules have reported for the transaction in question. Main memory controller 114 **compares the number of coherent transactions** responded to on lines 152 and 142 **against the number of coherent transactions listed in scoreboard 178** to determine the full/empty status of CCC queues 164 and 168."

If the **main memory controller 114** is incorporated into the same chip, as asserted in the Office Action, the Main memory controller 114 **could not compare the number of coherent transactions from all modules** against the number of coherent transactions listed in scoreboard 178 to determine the full/empty status of CCC queues 164 and 168. As clearly defined in MPEP 2143.02, it is well defined that "the prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success." *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The Applicants respectfully request

for traverse of the rejection because the Office Action fails to establish a reasonable expectation of success.

Thus, independent claim 1 is allowable over the prior art of record, and then its dependent claims 2-9 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 1 and further in view of the reasons set forth in the previous responses.

The rejection of claims 1-9, therefore, should be withdrawn.

Concerning the Rejection of Claims 10, 12, and 13 under 35 U.S.C. §103(a) as being unpatentable over Ziegler, in view of Handy

The Office Action has rejected Claims 10, 12 and 13 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Handy "The Cache Memory Book" (Handy).

In making the rejection, the Office Action correctly acknowledges that Ziegler neither discloses nor suggests a control chip includes a peripheral device interface controller and a data buffer, in view of the reasons set forth above. Furthermore, Ziegler neither discloses nor suggests the central processing unit uses a MOESI protocol, and "modified state" and "exclusive state" for the cache data stream, as addressed in claim 10.

There is no requisite teaching, suggestion or motivation to combine the teachings of means of "MOESI protocol" in the Handy with the Ziegler to render claim 10 obvious to people of ordinary skill in the art. Furthermore, neither of the references applied against claim 10, along or in combination, shows or suggests that "when the cache data stream is in a modified

state and if the data buffer executes a read operation from an address in memory that corresponds to the cache data stream, the peripheral device interface controller inform the central processing unit to set the cache data stream into an owner state; and when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address, the peripheral device interface controller will inform the central processing unit to set the cache data stream into a shared state", as addressed in claim 10.

Incorporated reasons of independent claim 10 being distinguished over Ziegler in view of Handy set forth above, the claim 10 is allowable over the prior art of record, then its dependent claims 12 and 13 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 10.

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CONCLUSION

For at least the foregoing reasons, it is believe that all pending claims 1-16 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,
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...for coating to all parts of the plant. (PE/EDPG) 422-1977

system enclosure (nuclear power generating station) ...cable penetration fire stops, fire breaks, and system enclosures) An assembly installed around a cable system to ...tain circuit integrity, for a specified time, of all circuits ...thin the enclosure when it is exposed to the most severe ...fire that may be expected to occur in the area. (PE/SUB/EDPG) 690-1984r, 525-1992r

cable terminal (1) A device that provides insulated egress for ...to the conductors. *Synonyms:* termination. (NESC) C2-1997 ...(2) (power work) A device that seals the end of a cable and provides insulated egress for the conductors. *Synonyms:* pothead; end bell. (PE/T&D) [10]

cable termination Parts assembled onto the end of the cable to ...provide the electrical and mechanical interface into the gas-insulated environment. Typically this includes a solid insulation barrier between the cable/cable fluid and the gas insulation of the GIS. (PE/IC) 1300-1996

cable tilt (loss) The amount of RF signal attenuation by a given coaxial cable. Cable attenuation is mainly a function of signal frequency, cable length, and diameter. Cables attenuate higher frequency signals more than lower frequency signals (dB). Cable losses are usually referenced to the highest frequency carried (greatest loss) on the cable. (LM/C) 802.7-1989r

cable tray (1) (raceway systems for Class 1E circuits for nuclear power generating stations) A prefabricated metal raceway with or without covers consisting of siderails and bottom support sections. Bottom support sections may be ladder, trough, or solid. (PE/NP) 628-1987r

(2) (electric power systems in commercial buildings) A unit or assembly of units or sections, and associated fittings, made of metal or other noncombustible material forming a continuous rigid structure used to support cables. (IA/PSE) 241-1990r

(3) A raceway resembling a ladder and usually constructed of metal. Other styles of trays include solid-bottom and channel type. (PE/IC) 848-1996

(4) A continuous rigid structure used to support cables. Cable trays include ladders, troughs, channels and other similar structures. Conduits are not included in this category. (PE/IC) 817-1993w

cable tray system (raceway systems for Class 1E circuits for nuclear power generating stations) An assembly of metallic cable tray sections, fittings, supports, anchorages, and accessories that form a structural system to support wire and cables. (PE/NP) 628-1987r

cable trolley *See:* cable car.

cable TV A communication system that simultaneously distributes several different channels of broadcast programs and other information to customers via a coaxial cable. Previously called community antenna television (CATV). (LM/C) 802.7-1989r

cable type (nuclear power generating station) A cable type for purposes of qualification testing shall be representative of those cables having the same materials, similar construction, and service rating, as manufactured by a given manufacturer. (PE/NP) 380-1975w

cable value *See:* manhole.

cab signal (1) A signal located in the enginemen's compartment or cab indicating a condition affecting the movement of a train or engine and used in conjunction with interlocking signals and in conjunction with or in lieu of block signals. *See also:* automatic train control. (EEC/PE) [119]

(2) (system) A signal located in the cab, indicating a condition affecting the movement of a train and used in conjunction with interlocking signals and in conjunction with or in lieu of block signals. (VT) 1475-1999

cache (1) A buffer inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. (C/BA) 895.3-1993w

(2) A small portion of high-speed memory used for temporary storage of frequently-used data, instructions, or operands. *See also:* instruction cache; disk cache; high-speed buffer; caching; cache architecture; data cache; cache memory. (C) 610.10-1994w

(3) *See also:* copy. (C/PA) 1328.2-1993w, 1224.2-1993w

cache coherence A system of caches is said to be coherent with respect to a cache line if each cache and main memory in the coherence domain observes all modifications of that same cache line. A modification is said to be observed by a cache when any subsequent read would return the newly written value. (C/BA) 1014.1-1994w, 10857-1994, 896.3-1993w, 896.4-1993w

cache agent A module that uses split transactions to assume all the rights and responsibilities of some number of remote cache modules. (C/BA) 896.4-1993w

cache line (1) Often called simply a "line." The unit of data on which coherence checks are performed, and for which coherence tag information is maintained. In SCI, a line consists of 64 data bytes. (MM/C) 1596-1992

(2) Often called simply a "line." The block of memory (sometimes called a "sector") that is managed as a unit for coherence purposes; i.e., cache tags are maintained on a per-line basis. SCI directly supports only one line size, 64 bytes. (C/MM) 1596.5-1993

(3) Often simply called a "line," the block of memory (sometimes called a sector) that is managed as a unit for coherence purposes; i.e., cache tags are maintained on a per-line basis. Although the SCI line size influenced the RamLink packet sizes, coherence protocols are beyond the scope of this standard. (C/MM) 1596.4-1996

cache architecture (A) A computer architecture that employs an extremely high-speed memory block, called a cache, in which data is stored. (B) The organization of cache memory; for example, direct mapped cache, two-way set associative cache. (C) 610.10-1994

cache hit *See:* hit.

caching The process of accessing a cache. (C) 610.10-1994w

cache memory (1) A buffer memory inserted between one or more processors and the bus, which is used to hold currently active copies of blocks of information from main memory. (C/BA) 1014.1-1994w

(2) A buffer memory inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. Cache memories exploit spatial locality by what is brought into a cache. Temporal locality is exploited by the strategy employed for determining what is removed from the cache. (C/BA) 10857-1994, 896.4-1993w

CAD *See:* computer-aided design.

CADD *See:* computer-aided design and drafting.

CADEM *See:* computer-aided engineering; computer-aided manufacturing; computer-aided design.

CADF *See:* commutated antenna direction finder.

CADM *See:* computer-aided manufacturing; computer-aided design.

CAE *See:* computer-aided engineering; computer-aided education.

cage (1) A system of conductors forming an essentially continuous conducting mesh or network over the object protected and including any conductors necessary for interconnection to the object protected and an adequate ground. *See also:* Faraday cage. (EEC/PE) [119]

(2) emptydef;. *See also:* aerial platform. (T&D/PE) 524-1992r

cage antenna A multi-wire element whose wires are so disposed as to resemble a cylinder, in general of circular cross section; for example, an elongated cage. (AP/ANT) 145-1993